EXHIBIT A

EXHIBIT A

Synopsys, Inc. v. Magma Design Automation, Inc.
(Case No. 05-701-GMS)

LIST OF AGREED UPON CLAIM TERM CONSTRUCTIONS

'508 Claim Term	Agreed Construction
fanins (Claim 11)	inputs to a circuit.
fanouts (Claims 9, 10)	terminals connected to the output of a gate.
gate (Claims 7-11)	a device having an output and one or more inputs, wherein the output is determined by the input, also referred to as a "cell."
initial placement (Claims 1-18)	a first placement of the integrated circuit elements of an integrated circuit, which can then be modified.
limits (Claims 1-18)	upper bounds.
logically equivalent (Claim 7)	performing the same logical function.
logic modification (Claims 1-18)	a modification of the actual logic of the circuit (as opposed to mere repositioning or trading places between gates).
modifying logic (Claims 4, 5, 7-11)	modifying the actual logic of the circuit (as opposed to mere repositioning or trading places between gates).

'508 Claim Term	**Agreed Construction**
net (Claims 12-14, 16, 18)	a connection between integrated circuit elements.
netlist (Claims 12-14, 16, 18)	a description of the connections between integrated circuit elements.
pin (Claim 8)	an input or an output of a gate. [Construction for the '508 and '328 patents only]
placement (Claims 1-18)	assigning the cells of the circuit to locations on the chip.
timing slack (Claim 5)	the degree to which a timing requirement is met in an integrated circuit design.
means for, subject to limits on the increase in area of integrated circuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design to allow congestion of the placement to be improved (Claim 17)	Construction of a portion of this phrase is governed by 35 U.S.C. § 112, ¶ 6. The claimed function is "performing logic modifications within selected bins of the integrated circuit design." The corresponding structure includes a computer executing algorithms for performing logic modifications within selected bins of the integrated circuit design, each logic modification including one of: 1. fanout splitting using buffering as shown in Figures 3A and 3B (*see* specification at col. 4, lines 23-45 and Figures 3A and 3B). In other words, adding buffers at the output pin of a gate and distributing the fanouts of the gate between the added buffers. 2. fanout splitting using node splitting as shown in Figures 3A and 3C (*see* specification at col. 4, lines 23-36 and 46-52, and Figures 3A and 3C). In other

'508 Claim Term	Agreed Construction
	words, replacing a gate with at least two copies of the gate, each of the copies fanning out to some of the fanouts of the gate. 3. intra-bin pin density logic optimization as shown in Figures 4A and 4B (*see* specification at col. 5, lines 1-12, and Figures 4A and 4B). In other words, replacing a set of gates in a bin with a different but logically equivalent set that has fewer pins. 4. input-splitting logic optimization as shown in Figures 4A, 4B, 6A and 6B (*see* specification at col. 5, lines 26-44, and Figures 4A, 4B, 6A and 6B). In other words, replacing a gate having a plurality of input pins with a set of gates, each one of which has fewer input pins. 5. Inter-bin pin density logic optimization as shown in Figures 5A and 5B (*see* specification at col. 5, lines 13-25, and Figures 5A and 5B). In other words, moving connections between gates and across bins to reduce pin density in a congested bin; and 6. performing logic modifications that speed up part of the circuit to improve timing slack in that part of the circuit, each logic modification including remapping or buffering (*see* Specification at col. 3, lines 65 through col. 4, line 7).
means, subject to limits on the increase in area of integrated circuit elements within a bin, performing logic modifications within selected bins of the integrated circuit design; wherein the logic modifications improve timing of selected nets belonging to the selected bins, reducing constraints on a subsequent placement step (Claim 18)	Construction of a portion of this phrase is governed by 35 U.S.C. § 112, ¶ 6. The claimed function is "performing logic modifications within selected bins of the integrated circuit design; wherein the logic modifications improve timing of selected nets belonging to the selected bins." The corresponding structure is a computer executing algorithms for: Performing logic modifications that speed up

'508 Claim Term	Agreed Construction
	part of the circuit to improve timing slack in that part of the circuit, each logic modification including either remapping or buffering. *See* Specification at col. 3, lines 65 through col. 4, line 7.

'328 Claim Term	Agreed Construction
active memory (Claims 11-13)	temporary data storage that can be read and changed while the computer is in use.
adapted (Claims 1-17)	suited.
area query (Claims 1-17)	a request for objects intersecting a specified area (synonymous with region query).
associated (Claims 1-17)	having a relationship with.
common data model (Claims 1-17)	a shared data model that does not require translation between the design tools.
data representation (Claims 1-17)	data objects, at least some of which stand for elements in an integrated circuit.
disk storage (Claim 13)	persistent storage by means of a disk.
logically correlated (Claims 1-17)	having a logical relationship.

'328 Claim Term	Agreed Construction
maintained (Claims 11, 12, 13)	kept.
net (Claim 9)	a connection between integrated circuit elements.
netlist (Claims 1-17)	a description of the connections between integrated circuit elements.
pin (Claim 10)	an input or an output of a gate. [Construction for the '508 and '328 patents only]
placement (Claim 15)	assigning the cells of the circuit to locations on the chip.

'745 Claim Term	Agreed Construction
bucket (Claims 1-8)	A rectangular, coarse placement region within the chip's core area. * "Placement region" means "a region on the chip's core defined before or during placement, into which cells have been or are later placed."
maintaining a congestion score for each bucket (Claims 1-8)	keeping or keeping up an adjusted congestion score during routing.
a range of congestion scores is equivalent to a given spacing configuration for wires in a bucket (Claim 6)	a given range of congestion scores corresponds to a particular spacing between wires in a bucket.

'745 Claim Term	Agreed Construction
when routing a wire through a bucket, modifying the congestion score accordingly (Claims 1-8)	every time a wire is routed through a bucket, modifying the congestion score accordingly.
routing (Claims 1-8)	interconnecting the components of the circuit with wiring.
lateral capacitance (Claim 8)	capacitance due to the overlap along the side walls of a wire with adjacent signal wires.

'116 Claim Term	Agreed Construction
netlist (Claims 1-52)	a description of the connections between integrated circuit elements.
prior integrated circuit (Claims 1-52)	an integrated circuit that has undergone the physical design phase.
pin (Claims 2, 10, 13, 14, 16, 24, 27-52)	a location at the edge of a block where a signal can enter the block or exit the block. [Construction for the '116 patent only]
pin assignment (Claims 2, 13, 14, 16, 27-52)	assignment of pin location.
using said netlist and said physical design information (Claims 8, 9, 22, 23, 29-52)	using the netlist and the physical design information for the purpose of improving the current integrated circuit
abutted-pin (Claims 10, 24, 38, 50)	pin(s) physically touching the edge or boundary of each block and resting against the edge or boundary of another block such that the pin(s) of one block abut(s) the pin(s) of another block.
hierarchical physical design (Claims 10, 24, 38, 50)	a physical design with two or more levels.
obstruction (Claims 11, 12, 25, 26, 36, 37, 48, 49)	an object or region in which further placement or routing is impeded
placement (Claims 13, 14, 27-52)	assigning the cells of the circuit to locations on the chip.
port (Claims 13, 14, 27-52)	an input or output internal to a block that may have connections to other ports in other blocks.

'116 Claim Term	Agreed Construction
to determine pin assignments (Claims 13, 14, 27-52)	to determine pin assignments for the current integrated circuit.
based on said top-level route (Claims 29-52)	using the top-level route for the purpose of improving pin assignments in the current integrated circuit
pressing (Claims 14, 28)	Removing the top-level objects within the boundary of a block from the top-level netlist and merging those objects into the block-level netlist of that block.

'093 Claim Term	Agreed Construction
pressing (Claims 1-40)	Removing the top-level objects within the boundary of a block from the top-level netlist and merging those objects into the block-level netlist of that block.
netlist (Claims 1-40)	a description of the connections between integrated circuit elements.
hierarchical state (Claims 1-40)	characterized by having at least two levels.
abutted-pin (Claims 2-4, 12-14, 22-24, 32-34)	pin(s) physically touching the edge or boundary of each block and resting against the edge or boundary of another block such that the pin(s) of one block abut(s) the pin(s) of another block.
hierarchical physical design (Claims 2-4, 12-14, 22-24, 32-34)	a physical design with two or more levels.
placement (Claims 21-40)	assigning the cells of the circuit to locations on the chip.

'093 Claim Term	Agreed Construction
press property (Claims 21-40)	a property of the top-level object that is stored, such that, if the property is present, the portion of the top-level object within the boundary of the block retains its location when pressed into the block, and, if the property is not present, the portion of the top-level object generally does not retain its location when pressed into the block.

'733 Claim Term	Agreed Construction
HDL (Claims 1-14)	abbreviation for "Hardware Description Language" – a computer language for a high-level description of an integrated circuit design
Netlist (Claims 1-26)	a description of the connections between integrated circuit elements
Partitioning information (Claims 1-26)	data representative of the sets of re-orderable scan cells
Clock domain (Claims 2, 9, 16, and 22-26)	a region of a circuit in which the timing behavior is identical or very similar
Edge sensitivity types (Claims 3, 10, 17, 22- 26)	the type of sensitivity of a cell (e.g., a rising edge sensitivity or a falling edge sensitivity or a positive edge or negative edge)
Reconfigurable multiplexer (Claims 4, 11, 18, and 24)	a switch used in a scan chain
Clock skew tolerance levels (Claims 5, 12 and 19)	the difference in time allowed between the arrival of the clock signals at two or more places (e.g., within an acceptable time window).
Surrounding cone logic (Claims 6, 13, 20, and 25)	a group of cells feeding a particular cell or being fed by a cell
Output switching times (Claims 7, 14, and 21)	the time at which a cell's output transitions to a given state
Scan chain (Claims 1-26)	scan cells connected together to form a chain or sequence

'733 Claim Term	Agreed Construction
Scan cells (Claims 1-26)	special memory cells specifically designed for test, which can be scanned

'501 Claim Term	Agreed Construction
Netlist (Claims 1-26)	a description of the connections between integrated circuit elements
Partitioning information (Claims 1-26)	data representative of the sets of re-orderable scan cells
Clock domain (Claims 2, 9, 16, 25, and 26)	a region of a circuit in which the timing behavior is identical or very similar
Edge sensitivity types (Claims 3, 10, 17, 25, and 26)	the type of sensitivity of a cell (e.g., a rising edge sensitivity or a falling edge sensitivity or a positive edge or negative edge)
Reconfigurable multiplexer (Claims 4, 11, 18, and 26)	a switch used in a scan chain
Clock skew tolerance levels (Claims 5, 12, 19, and 26)	the difference in time allowed between the arrival of the clock signals at two or more places (e.g., within an acceptable time window).
Surrounding cone logic (Claims 6, 13, 20, and 26)	a group of cells feeding a particular cell or being fed by a cell
Output switching times (Claims 7, 14, and 21)	the time at which a cell's output transitions to a given state
Scan chain (Claims 1-26)	scan cells connected together to form a chain or sequence
Scan cells (Claims 1-26)	special memory cells specifically designed for test, which can be scanned
Simultaneously switching output requirements (Claim 26)	limits to the number of output pins that can switch at one time

EXHIBIT B

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(Case No. 05-701-GMS)

U.S. Patent No. 6,192,508

'508 Patent Claims	Synopsys' Proposed Construction	Magma's Proposed Construction	Synopsys' Support	Magma's Support
bins (Claims 1-18)	one or more regions.	more than one bin.	**INTRINSIC EVIDENCE** Claim 1 preamble. (Col. 6, ll. 46-49). "It is important that the area used by the logic optimizations be monitored. Because the current placement (at the time of the logic optimizations) is based on a certain area of all the bins, if this information changes, then the placement may no longer be appropriate. The change may result in placement being done again at each step, and possibly the process never converging. Monitoring of the area used in order to preserve the feasibility of the placement is done by placing an upper bound on the area of each bin. The proposed logic optimizations are only allowed to increase the bin area to the upper bound. Bounding the increase in bin area guarantees convergence of the placement process." (Col. 5, ll. 58 – col. 6, ll. 2). "By the present amendment, the claims would be amended to account for the possibility of performing the present invention using only a single bin (i.e.,	**INTRINSIC EVIDENCE** 2:21-6:44 Figure 4a Claims 1-18 Amendment Under 37 C.F.R. § 312, dated March 6, 2000 (SYN1499155-158) in the '508 Patent Prosecution History (SYN1498962-SYN1499212). **EXTRINSIC EVIDENCE** Magma reserves the right to present expert opinion testimony by written declaration.

'508 Patent Claims	Synopsys' Proposed Construction	Magma's Proposed Construction	Synopsys' Support	Magma's Support
			one encompassing the entire integrated circuit) as opposed to multiple bins. This change is not believed to affect patentability of the claims. Entry of the amendment is respectfully requested." (SYN1499158). Amendment Under 37 C.F.R. § 312, dated March 6, 2000 (SYN1499155-158) in the '508 Patent Prosecution History (SYN1498962-SYN1499212). Response to Rule 312 Communication, dated May 9, 2000 (SYN1499159), in the '508 Patent Prosecution History (SYN1498962-SYN1499212). **EXTRINSIC EVIDENCE** "**region** *n. Abbr.* **reg. 1.** Any large, usually continuous segment of a surface or space; an area." *The American Heritage Dictionary of the English Language*, p. 1095 (William Morris, ed., Houghton Mifflin Co., 1976). Synopsys reserves the right to present expert opinion testimony by written declaration.	

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'508 Patent Claims	Synopsys' Proposed Construction	Magma's Proposed Construction	Synopsys' Support	Magma's Support
bin (Claims 1-15, 17, 18)	a region.	a rectangular (or square) portion of an integrated circuit bounded by gridlines.	Same evidence as cited for "**bins**."	**INTRINSIC EVIDENCE** 2:21-6:44 Claim 1 **EXTRINSIC EVIDENCE** "Application-Specific Integrated Circuits," Michael John Sebastian Smith, 1997, p. 882-885. Chang, *et.al.*, "Physical Hierarchy Generation with Routing Congestion Control," ISPD 2002. U.S. Patent No. 5,847,965. U.S. Patent No. 6,442,743. Magma reserves the right to present expert opinion testimony by written declaration.
in an attempt to improve congestion by taking advantage of the logic modifications (Claims 2-11, 13, 14)	to relieve congestion where opportunities are provided by logic modifications.	with the purpose of reducing congestion by taking advantage of more than one logic modification.	**INTRINSIC EVIDENCE** "The second method involves modifying the topology of the circuit by adding gates while maintaining the functionality, such that the added gates can then be moved by the placement steps to relieve congestion.	*See below* at "to allow congestion of the placement to be improved."

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'508 Patent Claims	Synopsys' Proposed Construction	Magma's Proposed Construction	Synopsys' Support	Magma's Support
			"An important aspect of the optimizations, specifically directed towards helping placement relieve congestion, is the ability to undo modifications if placement does not actually use the modifications. The undo capability ensures that no area/power resources are wasted for transformations the are not used as intended." (Col. 2, 43-52). "Modification of logic to potentially improve circuit congestion (Step 5). Techniques such as fanout splitting are used for this. "Placement modification to take advantage of the preceding modifications (Step 6)." (Col. 4, ll. 8-12). "For many of the congestion relieving logic synthesis methods proposed as part of placement, there are two important issues that this invention addresses. In most cases, logic synthesis cannot itself improve congestion, but rather only provide opportunities for placement to improve congestion, it is important to track which of these opportunities are	

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'508 Patent Claims	Synopsys' Proposed Construction	Magma's Proposed Construction	Synopsys' Support	Magma's Support
			actually used. Any unused opportunities may result in wasted resources, since the logic optimization step used to create them typically uses additional area and power (for faster cells) or additional gates. The use of the logic optimizations during placement is therefore actively tracked. Any unused optimizations are undone to ensure that there are no wasted resources." (Col. 5, ll. 45-57). **EXTRINSIC EVIDENCE** Synopsys reserves the right to present expert opinion testimony by written declaration.	
means for calculating congestion of the initial placement (Claims 17, 18)	Construction of this phrase is governed by 35 U.S.C. § 112, ¶ 6. The claimed function is "calculating congestion of the initial placement." The corresponding structure is a computer executing algorithms for: • calculating congestion for the initial placement using	Construction of this phrase is governed by 35 U.S.C. § 112, ¶ 6. The claimed function is calculating congestion of the initial placement. The corresponding structure is a computer executing algorithms for: calculating the total number of pins in the bin divided by the	**INTRINSIC EVIDENCE** Corresponding structure is found in the specification at: Figure 7 Col. 3, ll. 35-38 Col. 4, ll. 61-67 Col. 6, ll. 3-23 "Interconnection models for interconnects between bins and within bins provide both delay estimates for each interconnect in the circuit, as well as congestion estimates for each bin in	**INTRINSIC EVIDENCE** Fig. 7 4:61-63 6:3-23 **EXTRINSIC EVIDENCE** Magma reserves the right to present expert opinion testimony by written declaration.

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'508 Patent Claims	Synopsys' Proposed Construction	Magma's Proposed Construction	Synopsys' Support	Magma's Support
	interconnection models for interconnects between bins or within bins (Col. 3, ll. 35-38); or • calculating congestion for the initial placement in accordance with an algorithm that calculates the total number of pins in the bin divided by the total routable area in the bin (Col. 4, ll. 61-67).	total routable area in the bin.	the circuit." (Col. 3, ll. 35-38). "One measure of the congestion in a bin is given by pin density, calculated as the total number of pins in the bin divided by the total routable area in the bin. Here a pin refers to either an input of an output of a cell. It is desirable to get a lower congestion since that is likely to make routing easier. It is possible for logic optimizations to directly reduce this measure of congestion." (Col. 4, ll. 61-67). "Referring to FIG. 7, a diagram is shown of a computer system that may be used to practice the present invention." (Col. 6, ll. 12-13). **EXTRINSIC EVIDENCE** Synopsys reserves the right to present expert opinion testimony by written declaration.	
means for performing an initial placement of integrated circuit elements within bins on the design layout	Construction of this phrase is governed by 35 U.S.C. § 112, ¶ 6. The claimed function is "performing an initial placement	Construction of this phrase is governed by 35 U.S.C. § 112, ¶ 6. The claimed function is performing an initial placement	**INTRINSIC EVIDENCE** Corresponding structure is found in the specification at: Figure 7 Col. 3, ll. 31-35	**INTRINSIC EVIDENCE** None. **EXTRINSIC EVIDENCE**

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'508 Patent Claims	Synopsys' Proposed Construction	Magma's Proposed Construction	Synopsys' Support	Magma's Support
(Claim 17)	of integrated circuit elements within bins on the design layout." The corresponding structure is: • an electronic design automation placement tool; • a computer executing an algorithm for placing cells in one or more regions using a placement tool that partitions cells into one or more regions at each stage of the placement (Col. 3, ll. 31-35); and • a computer executing an algorithm for placing cells in accordance with a placement algorithm that is limited by the topology of the circuit (Col. 4, ll. 23-29).	of integrated circuit elements within bins on the design layout. The corresponding structure is: [No corresponding structure is disclosed.]	Col. 4, ll. 23-29 Col. 6, ll. 3-23 "The present invention may be used in conjunction with an electronic design automation placement tool. In accordance with an exemplary embodiment of one such placement tool, at each stage in cell placement, the cells are partitioned into a number of bins." (Col. 3, ll. 31-35). "Placement algorithms are limited in how they can place cells by the topology of the circuit. If the output of cell A is connected to (also referred to as 'fanning out to') four different terminals in different cells (indicated by the numbers 1-4) in FIG. 3(a), then the placement of A is strongly influenced by the placement of cells corresponding to these terminals." (Col. 4, ll. 23-29). "Referring to FIG. 7, a diagram is shown of a computer system that may be used to practice the present invention." (Col. 6, ll. 12-13). **EXTRINSIC EVIDENCE**	Magma reserves the right to present expert opinion testimony by written declaration.

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'508 Patent Claims	Synopsys' Proposed Construction	Magma's Proposed Construction	Synopsys' Support	Magma's Support
			Synopsys reserves the right to present expert opinion testimony by written declaration. Application-Specific Integrated Circuits, Michael John Sebastion Smith, © 1997 by Addison Wesley Longman, Inc., pp. 873-893.	
means for performing an initial placement of integrated circuit elements within bins on the design layout (Claim 18)	Construction of a portion of this phrase is governed by 35 U.S.C. § 112, ¶ 6. The claimed function is "performing an initial placement of integrated circuit elements within bins on the design layout." The corresponding structure is: • an electronic design automation placement tool; • a computer executing an algorithm for placing cells in one or more regions using a placement tool that partitions cells into one or more regions at each stage of the placement (Col. 3, ll. 31-35); and	Construction of a portion of this phrase is governed by 35 U.S.C. § 112, ¶ 6. The claimed function is performing an initial placement of integrated circuit elements within bins on the design layout. The corresponding structure is: [No corresponding structure is disclosed.]	**INTRINSIC EVIDENCE** Corresponding structure is found in the specification at: Figure 7 Col. 3, ll. 31-35 Col. 4, ll. 23-29 Col. 6, ll. 3-23 "The present invention may be used in conjunction with an electronic design automation placement tool. In accordance with an exemplary embodiment of one such placement tool, at each stage in cell placement, the cells are partitioned into a number of bins." (Col. 3, ll. 31-35). "Placement algorithms are limited in how they can place cells by the topology of the circuit. If the output of cell A is connected to (also referred to as 'fanning	*See above* at "means for performing an initial placement of integrated circuit elements within bins on the design layout."

'508 Patent Claims	Synopsys' Proposed Construction	Magma's Proposed Construction	Synopsys' Support	Magma's Support
	• a computer executing an algorithm for placing cells in accordance with a placement algorithm that is limited by the topology of the circuit (Col. 4, ll. 23-29).		out to') four different terminals in different cells (indicated by the numbers 1-4) in FIG. 3(a), then the placement of A is strongly influenced by the placement of cells corresponding to these terminals." (Col. 4, ll. 23-29). "Referring to FIG. 7, a diagram is shown of a computer system that may be used to practice the present invention." (Col. 6, ll. 12-13). **EXTRINSIC EVIDENCE** Synopsys reserves the right to present expert opinion testimony by written declaration. Application-Specific Integrated Circuits, Michael John Sebastion Smith, © 1997 by Addison Wesley Longman, Inc., pp. 873-893.	
reducing constraints on a subsequent placement step (Claims 12-14, 16, 18)	reducing one or more constraints on a subsequent placement step.	Plain meaning	**INTRINSIC EVIDENCE** "The circuit has timing constraints imposed on it that it needs to satisfy. The delay estimates of the interconnection, combined with the delays of the cells and the timing constraints imposed on the design, are	

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'508 Patent Claims	Synopsys' Proposed Construction	Magma's Proposed Construction	Synopsys' Support	Magma's Support
			converted to timing slack information for each part of the circuit. A negative timing slack indicates that that part of the circuit is not meeting the timing constraints. A positive slack indicates that that part of the circuit is producing its result faster that is needed and can thus be slowed down without violating its timing constraints. More generally, 'slack' is defined herein as a measure of the degree to which a timing requirement is met in an integrated circuit design. "The traditional role of logic synthesis has been to identify areas of the circuit which have negative timing slack and then modify the circuit so as to fix this problem. As described herein, logic synthesis is used to aid placement to achieve both acceptable delays and congestion, by making circuit modifications that increase the timing slack in the congested parts." (Col. 3, ll. 38-56). **EXTRINSIC EVIDENCE** Synopsys reserves the right to present expert opinion testimony by written declaration.	

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'508 Patent Claims	Synopsys' Proposed Construction	Magma's Proposed Construction	Synopsys' Support	Magma's Support
			See also the same evidence as cited for "**bins**."	
selected bins (Claims 1-18)	one or more selected regions.	more than one bin selected based on congestion.	Same evidence as cited for "**bins**."	**INTRINSIC EVIDENCE** 2:28-33 2:37-43 3:50-56 3:61-62 4:22-23 4:53-55 4:59-60 4:64-67 5:13-15 6:30-35 Fig. 2 Claims 1, 2, 3, 4, 17, and 18. Applicant Response, 1/20/2000, at 2, 3, 4. Notice of Allowability, 1/31/2000, at 2. **EXTRINSIC EVIDENCE** Magma reserves the right to present expert opinion testimony by written declaration.
to allow congestion of the placement to be	to provide opportunities for placement to improve congestion.	with the purpose of reducing congestion of the placement.	**INTRINSIC EVIDENCE** "The second method involves modifying	**INTRINSIC EVIDENCE** 2:21-22

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'508 Patent Claims	Synopsys' Proposed Construction	Magma's Proposed Construction	Synopsys' Support	Magma's Support
improved (Claims 1-11, 15, 17)			the topology of the circuit by adding gates while maintaining the functionality, such that the added gates can then be moved by the placement steps to relieve congestion. "An important aspect of the optimizations, specifically directed towards helping placement relieve congestion, is the ability to undo modifications if placement does not actually use the modifications. The undo capability ensures that no area/power resources are wasted for transformations the are not used as intended." (Col. 2, 43-52). "Modification of logic to potentially improve circuit congestion (Step 5). Techniques such as fanout splitting are used for this. "Placement modification to take advantage of the preceding modifications (Step 6)." (Col. 4, ll. 8-12). "For many of the congestion relieving logic synthesis methods proposed as part of placement, there are two important	2:28-33 2:47-52 3:50-56 3:65-4:7 4:13-14 4:22-23 4:59-60 4:64-67 5:45-57 6:30-35. Applicant Response, 1/20/2000, at 2, 3, 4. Notice of Allowability, 1/31/2000, at 2. **EXTRINSIC EVIDENCE** U.S. Patent No. 6,099,580. "Application-Specific Integrated Circuits," Michael John Sebastian Smith, 1997, ch. 16. "Physical Design CAD in Deep Sub-Micron Era," Mitsuhashi *et al.*, 1996, EURO-DAC '96. "Fanout-tree Restructuring Algorithm for Post-placement Timing Optimization," T. Aoki, 1995.

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'508 Patent Claims	Synopsys' Proposed Construction	Magma's Proposed Construction	Synopsys' Support	Magma's Support
			issues that this invention addresses. In most cases, logic synthesis cannot itself improve congestion, but rather only provide opportunities for placement to improve congestion, it is important to track which of these opportunities are actually used. Any unused opportunities may result in wasted resources, since the logic optimization step used to create them typically uses additional area and power (for faster cells) or additional gates. The use of the logic optimizations during placement is therefore actively tracked. Any unused optimizations are undone to ensure that there are no wasted resources." (Col. 5, ll. 45-57). "This invention will significantly reduce, if not eliminate, the iterations needed by considering not only the impact of interconnect during logic optimization of area/timing, but also at the same time doing logic optimization to help placement relieve congestion and thus generate a circuit that is easily routable." (Col. 6, ll. 30-35). **EXTRINSIC EVIDENCE** "**allow** *tr.v.* … **6.** To provide (the	Magma reserves the right to present expert opinion testimony by written declaration.

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'508 Patent Claims	Synopsys' Proposed Construction	Magma's Proposed Construction	Synopsys' Support	Magma's Support
			needed amount): *allow funds in case of emergency.*" *The American Heritage Dictionary of the English Language*, p. 35 (William Morris, ed., Houghton Mifflin Co., 1976). **EXTRINSIC EVIDENCE** Synopsys reserves the right to present expert opinion testimony by written declaration.	

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EXHIBIT C

Synopsys, Inc. v. Magma Design Automation, Inc.
(Case No. 05-701-GMS)

U.S. Patent No. 6,519,745

'745 Claim Terms	Synopsys' Proposed Construction	Magma's Proposed Construction	Synopsys' Support	Magma's Support
congestion score (Claims 1-8)	the ratio of routing resources used so far to the total routing resources available.	a ratio measure of routing resources.	**INTRINSIC EVIDENCE** "The congestion score for a bucket is defined as the ratio of the routing resources used so far to the total routing resources available in the bucket." '745 patent at 8:33-36. '745 patent at 3:63-4:3; 4:10-18; 8:17-9:29; Fig. 7; abstract. **EXTRINSIC EVIDENCE** Michael J.S. Smith, Application-Specific Integrated Circuits 859-861 (1997) U.S. Patent No. 6,618,846, at 5:53-57. Definition of "congest": "[t]o overfill or overcrowd." THE AMERICAN HERITAGE COLLEGE DICTIONARY 301 (4th ed. 2002). Synopsys reserves the right to present expert opinion testimony by written declaration.	**INTRINSIC EVIDENCE** 3:63-4:3 4:10-18 8:30-45 Fig. 7 Claim 2 **EXTRINSIC EVIDENCE** Expert opinion testimony by written declaration.

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EXHIBIT D

Synopsys, Inc. v. Magma Design Automation, Inc.
(Case No. 05-701-GMS)

U.S. Patent No. 6,857,116

'116 Claim Terms	Synopsys' Proposed Construction	Magma's Proposed Construction	Synopsys' Support	Magma's Support
generating said physical design (Claims 1-28)	producing an improved physical design for the current integrated circuit	**Plain meaning – no construction needed.**	**INTRINSIC EVIDENCE** "Thus, the software tools of the physical design phase 910 can customize the current integrated circuit to avoid the problems of the prior integrated circuit and to realize the benefits of the prior integrated circuit." '116 patent at 9:16-19. "By using physical design information 930 (concerning the block-level of the prior integrated circuit) at the top-level of the current integrated circuit, the decisions made at the top-level with respect to the top-level objects of the current integrated circuit will be able to reduce the problems present in the prior integrated circuit and will be able to generate solutions to overcome the problems present in the prior integrated circuit, improving the optimization of the abutted-pin hierarchical physical design	**INTRINSIC EVIDENCE** 2:23-60 6:64-7:7 7:26-58 7:66-8:-65 8:66-9:43 Amendment and Response to Office Action of February 3, 2003 Office Action of April 28, 2003 **EXTRINSIC EVIDENCE** "Generate, v.: . . . 3. To bring about, give rise to, produce." *Oxford English Dictionary* (2d. Ed. 1989). Expert opinion testimony by written declaration.

Synopsys, Inc. v. Magma Design Automation, Inc.
(Case No. 05-701-GMS)

'116 Claim Terms	Synopsys' Proposed Construction	Magma's Proposed Construction	Synopsys' Support	Magma's Support
			process of the present invention. Thus, if the physical design information 930 has information about several prior integrated circuits, the current integrated circuit is more likely to be optimized." '116 patent at 9:23-34. "In sum, the pin assignments generated with the use of the physical design information of the prior integrated circuit (FIGS. 10A-10C) were more optimal than the pin assignments generated without the use of the physical design information of the prior integrated circuit (FIGS. 10A-10C)." '116 patent at 10:53-57. "a method of improving a physical design of a current integrated circuit…." Preamble of claims 1, 15. '116 patent at 2:39-43; 8:8-30; 8:45-46; 8:58-11:22.	

Synopsys, Inc. v. Magma Design Automation, Inc.
(Case No. 05-701-GMS)

'116 Claim Terms	Synopsys' Proposed Construction	Magma's Proposed Construction	Synopsys' Support	Magma's Support
			Figs. 4-5, 8, 9B; 10A-C; 11A-C; 12A-C. Title of '116 patent. **EXTRINSIC EVIDENCE** Synopsys reserves the right to present expert opinion testimony by written declaration.	

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